Corrections to Fault Secure Encoder and Decoder for NanoMemory Applications

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This document is prepared as an attachment to [1], and its purpose is to correct the error in the presentation of a code in that paper. In [1] the code under consideration is a (15,7,5) EG-LDPC code. We used this code as an example to concretely illustrate the concept of the fault secure encoder, decoder, and checker; and the implementation of these units. There are a few representation errors in Figures 5, and 6 of paper [1] that we will correct in this document. The (15,7,5) EG-LDPC code has the generator polynomial

$$1 + x^4 + x^6 + x^7 + x^8. \tag{1}$$

This generator polynomial will result in the generator matrix, shown in Figure A below. We perform linear row operations to make this cyclic non-systematic generator matrix into systematic form. We perform the following operations:

$$i_0 = i_0 + i_4 + i_6 \tag{2}$$
$$i_1 = i_1 + i_5$$
$$i_2 = i_2 + i_6 \tag{3}$$

This systematic form is presented in Figure B. This is the correct representation of this systematic format and should replace Figure 5 of [1]. Based on this new generator matrix the encoder structure shown in Figure 6 of [1] will also need to be changed to the new encoder shown in Figure C.

	c_0	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}	c_{11}	c_{12}	c_{13}	c_{14}
i_0	1	0	0	0	1	0	1	1	1	0	0	0	0	0	0
i_1	0	1	0	0	0	1	0	1	1	1	0	0	0	0	0
i_2	0	0	1	0	0	0	1	0	1	1	1	0	0	0	0
i_3	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
i_4	0	0	0	0	1	0	0	0	1	0	1	1	1	0	0
i_5	0	0	0	0	0	1	0	0	0	1	0	1	1	1	0
i_6	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1

Figure A: The generator matrix of (15,7,5) EG-LDPC code in cyclic format

	c_0	c_1	c_2	c_3	c_4	c_5	c_6	c_7	c_8	c_9	c_{10}	c_{11}	c_{12}	c_{13}	c_{14}
i_0	1	0	0	0	0	0	0	1	0	0	0	1	0	1	1
i_1	0	1	0	0	0	0	0	1	1	0	0	1	1	1	0
i_2	0	0	1	0	0	0	0	0	1	1	0	0	1	1	1
i_3	0	0	0	1	0	0	0	1	0	1	1	1	0	0	0
i_4	0	0	0	0	1	0	0	0	1	0	1	1	1	0	0
i_5	0	0	0	0	0	1	0	0	0	1	0	1	1	1	0
i_6	0	0	0	0	0	0	1	0	0	0	1	0	1	1	1

Figure B: The generator matrix of (15,7,5) EG-LDPC code in systematic format

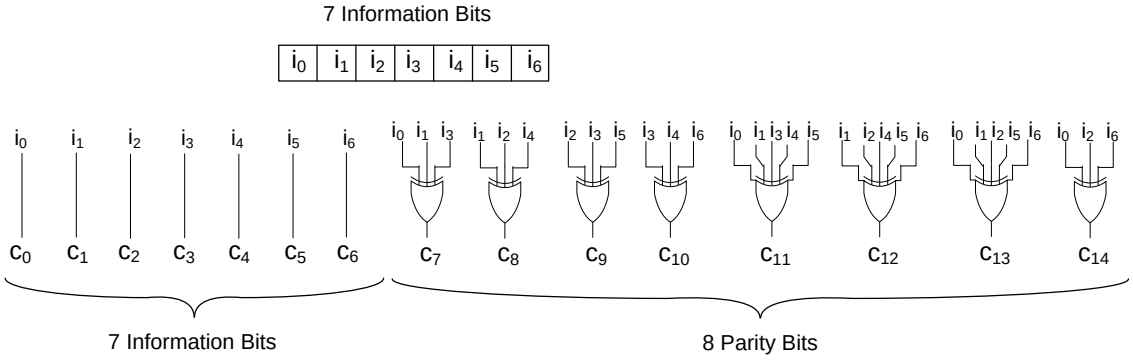

Figure C: The systematic encoder circuit of (15,7,5) EG-LDPC code

References

[1] Helia Naeimi. Fault Secure Encoder and Decoder for NanoMemory Applications. *IEEE Transaction on VLSI*, 17(4):473–486, April 2009.