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3D Nanowire-Based Programmable Logic

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***Abstract*— In nanowire-based logic, the semiconducting material (*e.g.*, Si, GaN, SiGe) is grown into individual nanowires rather than being part of the substrate. This offers us the opportunity to stack multiple layers of nanowires to create a three-dimensional logic structure which has high quality semiconductors in all vertical layers. We detail a feasible three-dimensional programmable logic architecture which can plausibly be realized from layers of semiconducting nanowires, making only modest assumptions about the control and placement of individual nanowires in the assembly. This shows a natural path for continuing to scale areal logic density once nanowire pitches approach fundamental limits. We show that the three dimensional systems are volumetrically efficient, with the surface area reducing roughly in proportion to the number of vertical layers. We further show that, on average, delay is reduced 18% from compact layout in three dimensions. For only a 20% area impact, we show how to avoid adding any manufacturing steps to physically isolate portions of nanowire layers.**

I. Introduction

Conventional, planar, lithographic processing has largely been limited to a single layer of high quality semiconductors. We grow the crystalline silicon at high temperatures, slice it into wafers, then process the surface of the wafer, leaving us with a single plane of good, active components. Metalization added for interconnect is not robust to the high temperatures required for crystalline silicon growth, preventing subsequent growth of high quality semiconductors on upper layers of a processed silicon wafer. Lower quality silicon can be deposited for use in memory (*e.g.*, [1]) and wafers can be processed separately and bonded together (*e.g.*, [2]).

In contrast, nanowires can be grown independently from the final substrate and later assembled onto the logic. Consequently, the bottom-up processes envisioned for nanowire construction allows us to separate the high temperature growth for the silicon from the lower temperature processing required for interconnect and assembly. We can grow good nanowires, then stack up numerous vertical layers, where each layer has high quality, crystalline semiconductors. Further, since the semiconductor is in the nanowires, we can potentially mix different semiconductor materials together into a single assembly (*e.g.*, Si, GaN, SiGe).

In this paper, we extend our planar nanoPLA architecture into three dimensions by showing how we can stack and connect additional layers of nanowires. This raises two key challenges:

1) How do we address individual nanowires which are stacked in vertical layers separated by only 10s of nanometers? (Sec. III)
2) How do we achieve the requisite vertical interconnect to allow communication between layers while simultaneously providing the necessary isolation for adjacent vertical layers to operate independently? (Sec. IV)

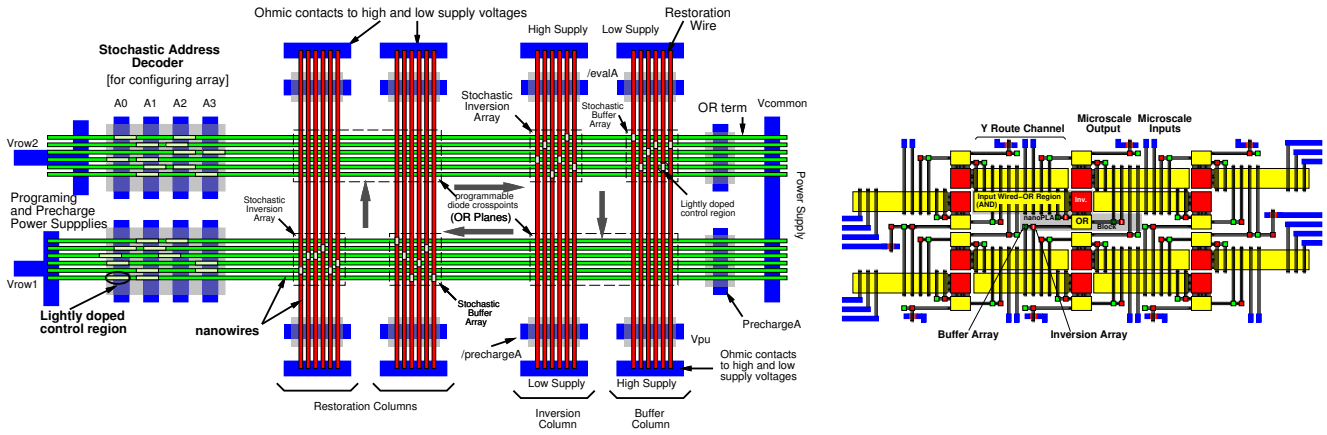
We extend our design mapping flow and analysis (Sec. V) to these three-dimensional architectures. This allows us to explore and quantify the density and delay benefits of the extended nanoPLA architectures (Sec. VI).

II. Background

A. Nanowires

Using seed catalysts (potentially created from self-limiting chemical processes (*e.g.*, [3])), semiconducting nanowires of a variety of materials (*e.g.*, Si [4], [5], Ge [4], GaAS, GaN [6], CdS, ZnS [7], TCNQ [8]), can be grown with controlled diameters down to 3 nm [4], [5]. The nanowires are high quality, single-crystal semiconductors with low resistance and high gain [9]. By material selection or doping, we can engineer the electrical properties of the nanowires (*e.g.*, P-type, N-type) [10]; one key control is the conduction threshold allowing the nanowire to be gated by an applied field [11]. The material composition or doping can be varied along the length of the nanowires to almost atomic precision [12]; this allows us to fabricate nanowires which are gateable in only select regions along their length. Further, we can control the material composition around the radius of the nanowire. This allows us to create core-shell hetrostructures [13], including semiconducting nanowires surrounded by insulating core shells which can be used to physically separate adjacent nanowires [14] or act as gate insulation for crossed field-effect gates.

Once grown and collected as individual nanowires, Langmuir-Blodgett (LB) flow techniques can be used to align a set of NWs into a single orientation, close pack them, and transfer them onto a surface [14], [15]. The resulting wires are all parallel with nematic alignment. By using wires with an oxide sheath around the conducting core, the wires can be packed tightly. The oxide sheath defines the spacing between conductors and can, optionally, be etched away after assembly. The LB step can be rotated and repeated so that we get



(a) Simple nanoPLA Block

(b) nanoPLA Block Tiling

Fig. 1. nanoPLA Organization

multiple layers of NWs [15], [16] such as crossed NWs for building a crossbar array or memory core. We can continue to repeat this alignment and transfer step to assemble vertical stacks composed of multiple layers of crossed nanowires.

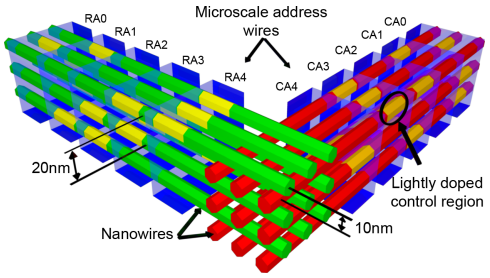
B. *nanoPLA*

Fig. 1(a) shows a simple nanoPLA organization [17] realized from two-layers of these crossed-nanowire building blocks. Features grown into the nanowires provide selectively gateable regions. As shown in Fig. 1(a), the simple array has two diode-programmable, wired-OR stages, each of which is followed by a stochastically assembled inversion and restoration stage. We can view the two stages as a NOR-NOR PLA or, by DeMorgan's Law, an AND-OR PLA.

The minimal arrangement in Fig. 1(a) demonstrates the key components of the nanoPLA but does not show how we get logical signals in to or out of the array. Fig. 1(b) shows how we adapt the nanoPLA computation strategy to build large-scale logic [18]. The restored nanowires are arranged to overlap adjacent nanoPLA blocks so that we get direct, nanoscale-density interconnect among nanoPLA blocks. This structure allows us to perform Manhattan routing to wire up connections between the nanoPLA logic blocks in a tiled array.

III. Nanowire Addressability

By growing nanowires with doping or material composition profiles along their axis, we can effectively give each nanowire an address. As illustrated in Fig. 1(a) (left side), each of the horizontal nanowires has a series of controllable (lightly doped) regions. By applying suitable voltages to the lithographic-scale crossed nanowires, we can selectively address nanowires that have a given control pattern and disable nanowires whose doping profile are not compatible with the voltages on the lithographic address wires. We have previously shown that, if we select a large enough address space, statistical assembly of the nanowires will leave each of the nanowires in a nanoPLA block with a virtually unique address [18], [19]; further, we can design the codes to tolerate the lack of end-to-end registration characteristic of nematic nanowire alignment [19]. While this method implies nanowire addresses are sparse and random, there is no need to permanently store the live nanowire address map for a PLA application; we can discover addresses during programming to configure the non-volatile crosspoints and discard this mapping once the device is configured.



Relative sizes and number of wires not shown to scale.

Fig. 2. Using Shared Address Conductors Across Nanowire Planes to Address Nanowires

For the three-dimensional nanoPLA, we stack additional nanowire layers. When each nanowire has a composite diameter, including shells, of around 10 nm, the distance between nanowires in parallel stacked planes is two layer heights or 20 nm. Consequently, we cannot rely on lithographic processing to individually connect to each of the stacked planes.

Fortunately, we do not actually need individual contacts from the lithographic scale to each of the planes. As the two-dimensional nanoPLA demonstrates, we can constrain our lithographic scale wires to contacting bundles of nanowires in a plane. For power supplies and gating, we connect groups of nanowires to a single contact. The key observation here is that the two-dimensional stochastic nanowire assembly solution extends to three dimensions. That is, if we arrange for the nanowires to have unique addresses across the different planes, then we need not contact the planes separately. We can, instead, use a thick conductor that connects simultaneously to the nanowires in multiple planes (See Fig. 2).

We could simply pick the size of the code space so that we have a suitably high probability of unique nanowire addresses across the set of N_z stacked planes. However, since we assemble each plane independently, we can deterministically use a disjoint set of nanowire addresses for each stacked layer. This reduces the required codespace by a factor of N_z ($100N_w^2N_z^2$ to $100N_w^2N_z$ for over 99% probability of unique addressibility [18]). An additional benefit of this scheme is that we know with which layer each nanowire address is associated. This means we know when two nanowires should interact because they are on adjacent, orthogonal layers and when they should be independent. As a result, this reduces the complexity of discovery and testing.

IV. Vertical Routing

To build our three-dimensional nanoPLA, we simply stack nanowire layers on top of each other. Think about taking the interconnected nanoPLA topology shown in Fig. 1(b) and stacking several copies (See also Fig. 3). The two-dimensional nanoPLA already operated by communicating between adjacent layers of nanowires. Programmable diode crosspoints between crossed, horizontal and vertical nanowires provided the programmable wired-OR planes (See Fig. 1(a)), and field-effect gating between crossed nanowires and lightly doped control regions on the adjacent layer provided restoration. The only difference as we go to additional stacked layers of nanowires is that each nanowire is now sandwiched between crossed nanowires that run both above it and below it.

A. $Z\pm$ Routing

A wired-OR nanowire can now be programmed to connect to any of the nanowires in the plane above it or the plane below it. Connections are programmed with voltage differentials just as before. As noted in the previous section, we can individually address each nanowire in a nanoPLA block, and we know which wires are in which layer based on their addresses. Consequently, we can apply a large voltage differential across a single junction between nanowires in the desired pair of layers. Since we can turn these programmable junctions off, we easily get layer isolation or connection as needed. If we think of each pair of orthogonal nanowire layers as a logical plane stack, then connection of the wired-OR input to the restoration nanowire above it constitutes an in-plane connection, consistent with the two-dimensional arrangement shown in Fig. 1(a); connections to the restoration nanowire below it will route a signal from plane Z to plane $Z+1$.

Each wired-OR nanowire is now sandwiched between the array of restoration nanowires in its own plane and the plane below it. Consequently, it can potentially field-effect gate **both** a restoration nanowire above it and below it. The ability to gate the restoration nanowire below it effectively allows a signal to be routed form plane Z to plane $Z-1$.

Unlike the wired-OR array, the restoration array is non-programmable. Without any additional care in manufacturing, each restoration nanowire can now be gated by both the nanowire above it (one in the $Z+1$ plane) and the nanowire below it (one in the Z plane). Consequently, we cannot independently restore wired-OR nanowires in adjacent layers.

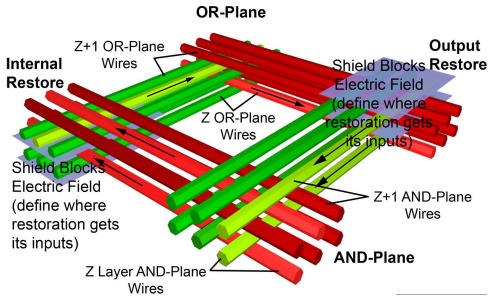


Fig. 3. Redefined Logical Nanowire Layer with Physical Isolation

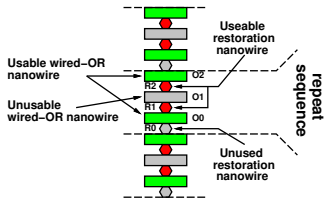


Fig. 4. Restoration Assignment Sequence which Allows us to Restore Two-Thirds of the Wired-OR Terms without Requiring any Physical Isolation

A manufacturing solution to this dilemma is to isolate one side of the restoration inputs. This allows us to independently restore each of the wired-OR nanowires. If that were all we did, we would lose the ability to route in the $Z-$ direction. To accommodate this, we redefine our nanoPLA plane as using restoration wires below it for the logical AND-plane and using restoration nanowires above it for the logical OR-plane (See Figs. 1(b) and 3). We use the logical AND plane for $Z+$ routing as before, and the OR-plane for $Z-$ routing.

Alternatively, a logical solution to this problem is to accept that we cannot independently restore the two nanowires and simply demand that we use every other nanowire. That is, half of the wired-OR nanowires in each plane are simply programmed into a non-controlling stage (*e.g.*, a low voltage for depletion mode, P-type restoration nanowires) so that only one of the wired-OR nanowires adjacent to each restoration wire is active. We alternate the placement of used and unused wires in arrays. The net effect is that we must place twice as many wired-OR nanowires as we actually use.

With clever assignment, we can independently use at least two thirds of the wired-OR terms which are aligned in a stack. In particular, we can independently restore two of every three aligned wired-OR terms as shown in Fig. 4. Here, R1 restores O0 and R2 restores O2. O1 is left unused to avoid interfering with R1 or R2. R0 ends up gated by both O0 and the O3 in an adjacent copy of the sequence; the wire will toggle, but we avoid ever using the output it produces.

B. Interaction with Stochastic Restoration

The simplest manufacturing scheme for the restoration array relies on stochastic population of the restoration nanowires [18]. As shown in Fig. 1(a), not all of the wires will be restored

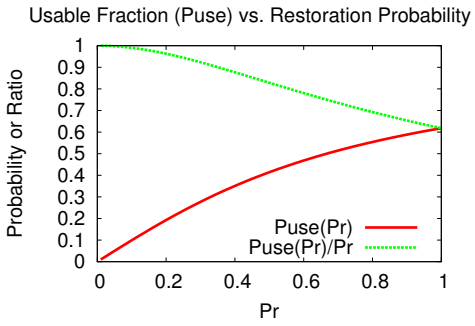


Fig. 5. P_{use} as a Function of P_r

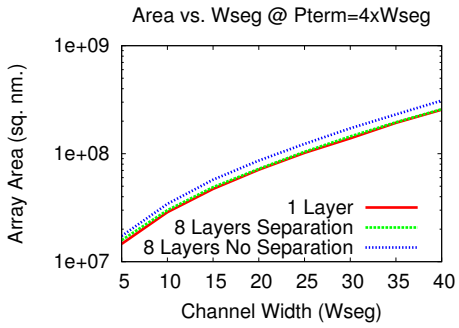


Fig. 6. Area Impact of No Physical Separation

in a given restoration array. In the right side inversion column, the fourth wired-OR nanowire from the top is not restored, while the fifth nanowire is restored twice. This means that not all of the wired-OR nanowires would be used even if we had perfect isolation. The consequence is that we will have cases where a restoration array does not provide restoration for a particular wired-OR nanowire position.

The key observation to make here is that non-usability of wired-OR nanowires is not simply the sum of the non-usability due to stochastic population effects and non-usability due to overlap. In particular, we can often assign wires so that the required non-used restoration wires (*e.g.*, R0 in Fig. 4) are allocated to stochastically non-restored position in the array.

Let P_r be the probability a particular input position to the restoration array in a particular plane is restored. Following the restoration assignment scheme shown in Fig. 4, we can conclude that a particular restoration nanowire can be used only if it is providing a non-redundant restoration in its plane (*i.e.*, P_r) and at least one of the two restoration nanowires in planes immediately below it is not being used; this last requirement makes sure that we skip one nanowire in every group of three to provide separation as detailed above. Let P_{use_i} be the probability that the nanowire in plane i is usable, then we can compute P_{use_i} as a recurrence relation:

$$P_{use_i} = P_r \times \left(1 - P_{use_{i-1}} \times P_{use_{i-2}}\right) \tag{1}$$

For a large number of layers, P_{use_i} should converge to a fixed point, P_{use}. Solving for P_{use}, we get:

$$P_{use} = \frac{\left(\sqrt{(4P_r^2 + 1)} - 1\right)}{2P_r} \tag{2}$$

The result is plotted in Fig. 5.

The overall area impact for no separation is modest (20%) as shown in Fig. 6. This comes in part because the typical P_r is around 60%, where $P_{use}/P_r \approx 80\%$ (See Fig. 5), and in part because of the fixed lithographic support overhead whose area does not change as the number of raw PTERMs increases.

V. CAD Flow

Our basic CAD mapping flow follows the standard interconnected nanoPLA mapping flow from [18]. Designs are optimized with `sis` [20], then covered to single-output PLA

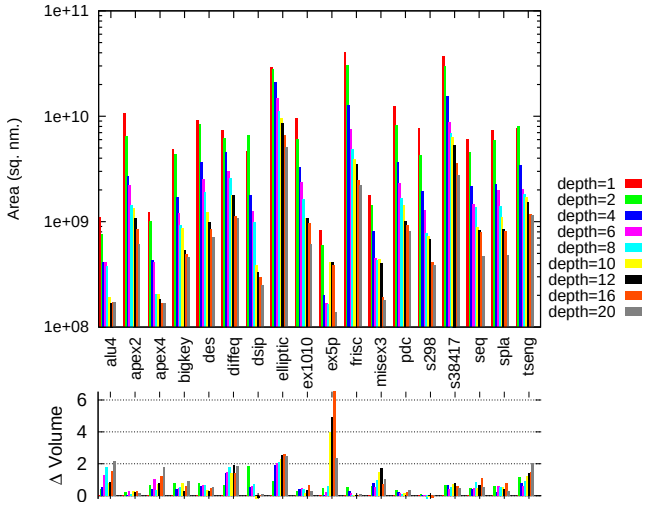


Fig. 7. Two-Dimensional Area versus Depth

covers with bounded number of inputs and PTERMs using PLAMAP [21]. The single-output covers are grouped into nanoPLA block feasible clusters with limited inputs (I), PTERM (P), and outputs (O) using a greedy packer similar to `vpack` [22] but aware of the PTERMs required for each output. Blocks are then placed with TPR 1.0 alpha [23], [24]. For the depth=1 cases, we use VPR 4.3 [22] for placement. For routing, we extended our nanoPLA router (`npr`) [18] to support multiple layers and connections between layers.

VI. Results

Mapping designs from the Toronto20 benchmark set [25], Fig. 7 shows how two-dimensional area decreases with additional layers (depth) for the no separation case. The bottom of Fig. 7 plots:

$$\Delta\text{Volume} = \frac{area \times depth}{area2d} - 1 \tag{3}$$

Fig. 7 suggests we lose some volumetric efficiency going from depth=1 to 2, but volume is fairly constant after that step; inefficiency arises primarily from packing granularity and no separation effects.

The compact layout in three dimensions reduces the worst-case distance across N nanoPLA blocks from $2\sqrt{N}$ to $3\sqrt[3]{N}$. The net effect on critical path is shown Table I. Here we see

TABLE I

RELATIVE DISTANCE DELAY VS. DEPTH

	Best		Relative TPR Delay at Depth				
name	Ratio	Depth	1	2	4	6	8
alu4	0.90	4	1.30	1.30	0.90	1.10	1.80
apex2	0.66	10	1.27	1.12	0.76	0.76	0.66
apex4	0.85	5	1.08	0.92	1.08	0.92	0.92
bigkey	0.87	6	1.40	1.07	0.93	0.87	1.13
des	1.00	1	1.53	1.33	1.10	1.03	1.17
diffeq	1.00	1	1.39	1.13	1.39	1.26	1.22
dsip	0.93	4	1.36	1.07	0.93	1.00	1.14
elliptic	0.79	7	0.97	1.09	0.94	0.79	0.87
ex1010	0.54	6	1.04	0.85	0.72	0.54	0.59
ex5p	0.60	3	1.10	1.00	0.70	0.70	0.80
frisc	0.80	11	1.08	1.08	0.98	0.89	0.85
misex3	0.88	4	1.12	1.00	0.88	1.12	0.94
pdc	0.84	6	1.43	1.14	0.86	0.84	0.86
s298	0.77	6	1.18	1.03	0.98	0.77	0.97
s38417	0.83	9	1.08	1.27	0.98	0.92	0.96
seq	0.88	9	1.31	1.27	0.92	1.00	0.96
spla	0.81	11	1.10	1.16	0.90	0.97	0.94
tseng	1.00	1	1.30	1.13	1.26	1.13	1.13
	0.82		Geometric Mean				

All ratios are to the single layer (depth 1) delay from VPR.

the best layer choices for some designs cut their routing almost in half. On average, designs reduce the number of routing hops by 18%. TPR does not optimize placement for delay as well as VPR (as shown in Table I), so we expect this can be improved.

VII. OPEN

An important area of future work is to explore energy-area tradeoffs. In particular, if we are power-density limited, then we can afford to sacrifice some area to reduce the energy of a computation, and hence increase the computational-density delivered by a power-density-limited system. These three-dimensional designs increase the likelihood we will be power-density limited, but they also give us more capacity with which to work as we find ways to exploit energy-area tradeoffs.

VIII. CONCLUSIONS

Nanowire-based logic arrays can be extended to three-dimensional structures exploiting high quality nanowires of a variety of materials in each of the layers. The nanowires can be independently addressed in each layer without further complicating fabrication. Signals can be routed between adjacent, stacked layers and, using the wire assignment discipline we introduce, signals can be isolated and restored from a single layer as appropriate. This gives us a path to continue to scale effective areal logic density beyond the point where nanowire diameters and pitches reach physical and electrical limits.

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